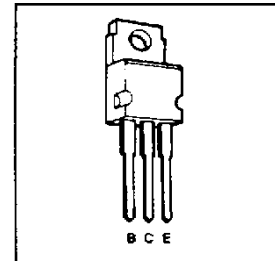


**TIP120, TIP121, TIP122**  
**NPN DARLINGTON - CONNECTED**  
**SILICON POWER TRANSISTORS**

SLPS054 Revised March 1990

- Designed for Complementary Use with TIP125, TIP126 and TIP127
- 65 W at 25°C Case Temperature
- 5 A Continuous Collector Current
- Min  $h_{FE}$  of 1000 at 3 V, 3 A
- Designed for Ignition Systems, Motor Control and Solenoid Driver Applications



PACKAGE: TO220

**Absolute Maximum Ratings at 25°C Case Temperature (unless otherwise noted)**

		TIP120	TIP121	TIP122
$V_{CE0}$	Collector - base voltage ( $I_E = 0$ )	60 V	80 V	100 V
$V_{CE0}$	Collector - emitter voltage ( $I_B = 0$ )	60 V	80 V	100 V
$V_{EB0}$	Base - emitter voltage		5 V	
$I_C$	Continuous collector current		5 A	
$I_{CM}$	Peak collector current (Note 1)		8 A	
$I_B$	Continuous base current		0.1 A	
$P_{Tot}$	Continuous device dissipation at (or below) 25°C case temperature (Note 2)		65 W	
$P_{Tot}$	Continuous device dissipation at (or below) 25°C free - air temperature (Note 3)		2 W	
$I_C^2 L/2$	Unclamped inductive load energy (Note 4)		50 mJ	
$T_J$ & $T_{Stg}$	Operating junction and storage temperature range	-65°C to +150°C		
$T_L$	Lead temperature 3.2 mm from case for 10 seconds	260°C		

NOTES: 1. This value applies for  $t_w \leq 0.3$  ms, duty cycle  $\leq 10\%$   
 2. Derate linearly to 150°C case temperature at the rate of 0.52 W/°C  
 3. Derate linearly to 150°C free - air - temperature at the rate of 16 mW/°C  
 4. This rating is based on the capability of the transistors to operate safely in a circuit of:  $L = 20$  mH,  $R_{ESR} = 100 \Omega$ ,  $V_{CE} = 0$  V,  $R_{\theta} = 0.1 \Omega$ ,  $V_{CC} = 20$  V Energy =  $I_C^2 L/2$

**Electrical Characteristics at 25°C Case Temperature (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(BR)CEO}$	Collector - emitter sustaining voltage $I_C = 30$ mA $I_B = 0$ (Note 5)	TIP120 60 TIP121 80 TIP122 100			V
$I_{CEO}$	Collector - emitter cut - off current $V_{CE} = 30$ V $I_B = 0$ TIP120 $V_{CE} = 40$ V $I_B = 0$ TIP121 $V_{CE} = 50$ V $I_B = 0$ TIP122			0.5 0.5 0.5	mA
$I_{CBO}$	Collector cut - off current $V_{CB} = 60$ V $I_E = 0$ TIP120 $V_{CB} = 80$ V $I_E = 0$ TIP121 $V_{CB} = 100$ V $I_E = 0$ TIP122			0.2 0.2 0.2	mA
$I_{EBO}$	Emitter cut - off current $V_{EB} = 5$ V $I_C = 0$			2	mA
$h_{FE}$	Forward current transfer ratio $V_{CE} = 3$ V $I_C = 0.5$ A (Notes 5 & 6) $V_{CE} = 3$ V $I_C = 3$ A	1000 1000			
$V_{CE(sat)}$	Collector - emitter saturation voltage $I_B = 4$ mA $I_C = 3$ A (Notes 5 & 6) $I_B = 20$ mA $I_C = 5$ A			2 4	V
$V_{BE}$	Base - emitter voltage $V_{CE} = 3$ V $I_C = 3$ A (Notes 5 & 6)			2.5	V
$V_F$	Parallel diode forward voltage $I_F = -I_C = 5$ A $I_B = 0$ (Notes 5 & 6)			3.5	V

# TIP120, TIP121, TIP122 NPN DARLINGTON - CONNECTED SILICON POWER TRANSISTORS

## Thermal Characteristics

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction - to - case thermal resistance			1.92	$^{\circ}\text{C}/\text{W}$
$R_{\theta JA}$	Junction - to - free - air thermal resistance			62.5	$^{\circ}\text{C}/\text{W}$

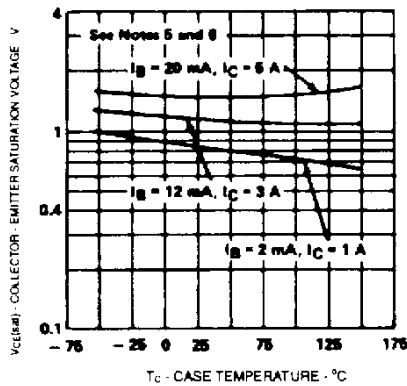
## Resistive - Load - Switching Characteristics at 25 $^{\circ}\text{C}$ Case Temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>†</sup>			MIN	TYP	MAX	UNIT
$t_{on}$	Turn on time	$I_C = 3 \text{ A}$	$I_{B(on)} = 12 \text{ mA}$ $I_{B(off)} = -12 \text{ mA}$		1.5		$\mu\text{s}$
$t_{off}$	Turn off time	$V_{BE(off)} = -5 \text{ V}$	$R_L = 10 \Omega$		8.5		$\mu\text{s}$

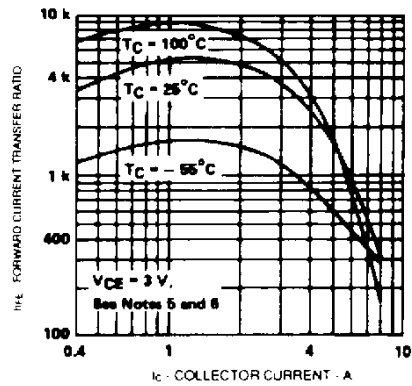
<sup>†</sup> Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.  
 NOTES: 5. These parameters must be measured using pulse techniques,  $t_w = 300 \mu\text{s}$ , duty cycle  $\leq 2\%$ .  
 6. These parameters must be measured using voltage sensing contacts separate from the current-carrying contacts.

## TYPICAL CHARACTERISTICS

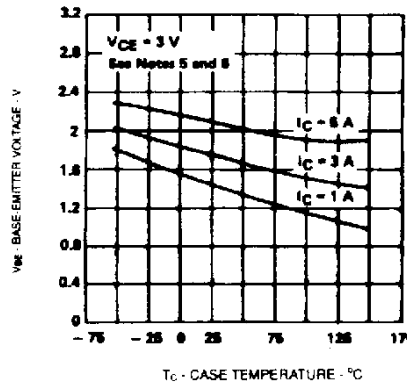
COLLECTOR - EMITTER SATURATION VOLTAGE  
vs  
CASE TEMPERATURE



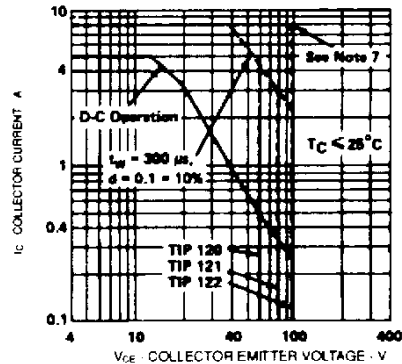
FORWARD CURRENT TRANSFER RATIO  
vs  
COLLECTOR CURRENT



BASE-EMITTER VOLTAGE  
vs  
CASE TEMPERATURE



MAXIMUM FORWARD - BIAS  
SAFE OPERATING AREA



NOTE: 7 This combination of maximum voltage and current may be achieved only when switching from saturation to cutoff with a damped inductive load.



## **IMPORTANT NOTICE**

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

**TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.**

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.